## SILICON MMIC 2.0 GHz FREQUENCY UP-CONVERTER FOR CELLULAR TELEPHONE

## DESCRIPTION

The $\mu \mathrm{PC} 8163 \mathrm{~TB}$ is a silicon monolithic integrated circuit designed as frequency up-converter for cellular telephone transmitter stage. The $\mu$ PC8163TB has improved intermodulation performance and smaller package.

The $\mu$ PC8163TB is manufactured using NEC's $20 \mathrm{GHz} \mathrm{ft}^{\mathrm{NESAT}}{ }^{\top M}{ }^{\text {IIII }}$ silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

## FEATURES

- Recommended operating frequency : frFout $=0.8 \mathrm{GHz}$ to 2.0 GHz , fifin $=50 \mathrm{MHz}$ to 300 MHz
- Supply voltage
: $\mathrm{Vcc}=2.7$ to 3.3 V
- High-density surface mounting
: 6-pin super minimold package
- Higher IP3
$: \mathrm{OIP}_{3}=+9.5 \mathrm{dBm} @ \mathrm{frFout}=830 \mathrm{MHz}$
- Minimized carrier leakage
: Due to double balanced mixer


## APPLICATIONS

- Digital cellular phones


## ORDERING INFORMATION

| Part Number | Package | Supplying Form |
| :---: | :---: | :--- |
| $\mu$ PC8163TB-E3 | 6-pin super minimold | Embossed tape 8 mm wide. <br> Pin 1, 2, 3 face to tape perforation side. <br> Qty 3 kp/reel |

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: $\mu$ PC8163TB)

## Caution Electro-static sensitive device

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

## PIN CONNECTIONS



| Pin No. | Pin Name |
| :---: | :---: |
| 1 | IFinput |
| 2 | GND |
| 3 | LOinput |
| 4 | GND |
| 5 | Vcc |
| 6 | RFoutput |

SERIES PRODUCTS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\text {RFout }}=3.0 \mathrm{~V}, \mathrm{ZL}_{\mathrm{L}}=\mathrm{Z}_{\mathrm{s}}=50 \Omega\right.$ )

| Type | Part No. | $\mathrm{Vcc}(\mathrm{V})$ | Icc <br> $(\mathrm{mA})$ | CG 1 <br> $(\mathrm{~dB})$ | CG 2 <br> $(\mathrm{~dB})$ | $\mathrm{Po}($ sat) 1 <br> $(\mathrm{dBm})$ | $\mathrm{Po}($ sat) 2 <br> $(\mathrm{dBm})$ | $\mathrm{OIP}_{3} 1$ <br> $(\mathrm{dBm})$ | $\mathrm{OIP}_{3} 2$ <br> $(\mathrm{dBm})$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| High $\mathrm{IP}_{3}$ | $\mu \mathrm{PC} 8106 \mathrm{~TB}$ | 2.7 to <br> 5.5 | 9 | 9 | 7 | -2 | -4 | +5.5 | +2.0 |
| Low Power Consumption | $\mu \mathrm{PC} 8109 \mathrm{~TB}$ | 2.7 to <br> 5.5 | 5 | 6 | 4 | -5.5 | -7.5 | +1.5 | -1.0 |
| Higher IP 3 |  |  |  |  |  |  |  |  |  |

## Caution The above table lists the typical performance of each model. See ELECTRICAL CHARACTERISTICS for the test conditions.

BLOCK DIAGRAM (FOR THE $\mu$ PC8163TB)


SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEM)


## PIN EXPLANATION

| Pin <br> No. | Pin <br> Name | Applied <br> Voltage <br> V | Pin <br> Voltage <br> $V^{\text {Note }}$ | Function and Explanation |
| :---: | :---: | :---: | :---: | :--- | :--- |
| 1 | IFinput | - | 1.2 | This pin is IF input to double balanced mixer <br> (DBM). The input is designed as high <br> impedance. The circuit contributes to <br> suppress spurious signal. Also this <br> symmetrical circuit can keep specified <br> performance insensitive to process-condition <br> distribution. For above reason, double <br> balanced mixer is adopted. |
| 2 | GND | 0 | - | GND pin. Ground pattern on the board <br> should be formed as wide as possible. <br> Track Length should be kept as short as <br> possible to minimize ground impedance. |
| 4 | LOinput | - | 2.1 | Local input pin. Recommendable input level <br> is -10 to 0 dBm. |
| 5 | Vcc | 2.7 to 3.3 | - | Supply voltage pin. |
| 6 | RFoutput | Same <br> bias as <br> Vcc <br> through <br> external <br> inductor | - | This pin is RF output from DBM. This pin is <br> designed as open collector. Due to the high <br> impedance output, this pin should be <br> externally equipped with LC matching circuit <br> to next stage. |

Note Each pin voltage is measured with $\mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\mathrm{RF}}$ out $=3.0 \mathrm{~V}$.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Test Conditions | Rating | Unit |
| :--- | :---: | :--- | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{cc}}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, Pin 5 and 6 | 3.6 | V |
| Power Dissipation of Package | PD | Mounted on double-sided copperclad $50 \times 50 \times 1.6$ <br> mm epoxy glass PWB <br> $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ | 200 | mW |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ |  | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Input Power | $\mathrm{P}_{\text {in }}$ |  | +10 | dBm |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage | Vcc | The same voltage should be applied to pin 5 and 6 | 2.7 | 3.0 | 3.3 | V |
| Operating Ambient Temperature | TA |  | -40 | +25 | +85 | ${ }^{\circ} \mathrm{C}$ |
| Local Input Level | PLoin | Zs = $50 \Omega$ (without matching) | -10 | -5 | 0 | dBm |
| RF Output Frequency | frout | With external matching circuit | 0.8 | - | 2.0 | GHz |
| IF Input Frequency | fiFin |  | 50 | - | 300 | MHz |

## ELECTRICAL CHARACTERISTICS

$\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\text {RFout }}=\mathbf{3 . 0} \mathrm{V}\right.$, fifin $=150 \mathrm{MHz}, \mathrm{P}_{\text {LOin }}=-5 \mathrm{dBm}$ )

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Circuit Current | Icc | No Signal | 11.5 | 16.5 | 23 | mA |
| Conversion Gain 1 | CG1 | $\mathrm{ffFout}=830 \mathrm{MHz}$, $\mathrm{PlFin}=-20 \mathrm{dBm}$ | 6 | 9 | 12 | dB |
| Conversion Gain 2 | CG2 | $\mathrm{ffFout}=1.9 \mathrm{GHz}, \mathrm{P}_{\text {IFin }}=-20 \mathrm{dBm}$ | 2.5 | 5.5 | 8.5 | dB |
| Maximum RF Output Power 1 | Po (sat) 1 | $f_{\text {RFout }}=830 \mathrm{MHz}$, $\mathrm{PlFin}=0 \mathrm{dBm}$ | -1.5 | 0.5 | - | dBm |
| Maximum RF Output Power 2 | Po (sat) 2 | $\mathrm{ffFout}=1.9 \mathrm{GHz}, \mathrm{PlFin}=0 \mathrm{dBm}$ | -4.5 | -2 | - | dBm |

## OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY

( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{Cc}}=\mathrm{V}_{\text {RFout }}=3.0 \mathrm{~V}, \mathrm{P}_{\text {LOin }}=-5 \mathrm{dBm}$ )

| Parameter | Symbol | Conditions |  | Data | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Third Order Distortion Intercept Point | $11 \mathrm{P}_{3} 1$ | $\begin{aligned} & \mathrm{flFin} 1=150.0 \mathrm{MHz} \\ & \mathrm{f}_{\text {IFin2 }}=150.4 \mathrm{MHz} \end{aligned}$ | $\mathrm{fRFout}^{\text {f }}$ 830 MHz | 0.5 | dBm |
|  | IIP 3 |  | $\mathrm{f}_{\text {RFout }}=1.9 \mathrm{GHz}$ | 0.5 |  |
| Output Third-Order Distortion Intercept Point | $\mathrm{OIP}_{3} 1$ | $\begin{aligned} \mathrm{flFin} 1 & =150.0 \mathrm{MHz} \\ \mathrm{fl}_{\text {IFin2 }} & =150.4 \mathrm{MHz} \end{aligned}$ | $\mathrm{ffFout}^{\text {a }}$ 830 MHz | +9.5 | dBm |
|  | $\mathrm{OIP}_{3} 2$ |  | $\mathrm{f}_{\text {frout }}=1.9 \mathrm{GHz}$ | +6.0 |  |
| SSB Noise Figure | SSB NF | $\mathrm{ffFout}=830 \mathrm{MHz}$, $\mathrm{flFin}^{\text {a }}=150 \mathrm{MHz}$ |  | 12.5 | dB |

## TEST CIRCUIT 1 (frfout $=830 \mathrm{MHz}$ )



## ILLUSTRATION OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



## EVALUATION BOARD CHARACTERS

(1) $35 \mu \mathrm{~m}$ thick double-sided copper clad $35 \times 42 \times 0.4 \mathrm{~mm}$ polyimide board
(2) Back side: GND pattern
(3) Solder plated patterns
(4) ○O: Through holes

ATTENTION Test circuit or print pattern in this sheet is for testing IC characteristics.
In the case of actual system application, external circuits including print pattern and matching circuit constant of output port should be designed in accordance with IC's S parameters and environmental components.

## TEST CIRCUIT 2 (fRFout $=1.9 \mathrm{GHz}$ )



## ILLUSTRATION OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



EVALUATION BOARD CHARACTERS
(1) $35 \mu \mathrm{~m}$ thick double-sided copper clad $35 \times 42 \times 0.4 \mathrm{~mm}$ polyimide board
(2) Back side: GND pattern
(3) Solder plated patterns
(4) $\circ$ O: Through holes
$\star$ TYPICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise specified $\mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\mathrm{rFout}}$ )

$\star$ S-PARAMETER FOR MATCHED RF OUTPUT (Vcc = VrFout $=3.0 \mathrm{~V}$ ) - with TEST CIRCUITS 1 and 2 (monitored at RF connector on board)

- RF output matched at 830 MHz


- RF output matched at 1.9 GHz


START $100.000000 \mathrm{MHz} \quad$ STOP 3000.000000 MHz


## 

LO port


RF port (no matching)


IF port




CONVERSION GAIN vs. LO INPUT LEVEL


CONVERSION GAIN vs. LO INPUT LEVEL



CONVERSION GAIN vs. IF INPUT FREQUENCY


CONVERSION GAIN vs. IF INPUT FREQUENCY


CONVERSION GAIN vs. IF INPUT FREQUENCY



RF OUTPUT LEVEL vs. IF INPUT LEVEL


RF OUTPUT LEVEL OF EACH TONE AND IM3 vs. IF INPUT LEVEL


RF OUTPUT LEVEL vs. IF INPUT LEVEL


RF OUTPUT LEVEL vs. IF INPUT LEVEL


RF OUTPUT LEVEL OF EACH TONE AND IM 3 vs. IF INPUT LEVEL



IF Input Level PIFin (dBm)

LO LEAKAGE AT IF PIN vs. LO INPUT FREQUENCY


LO LEAKAGE AT RF PIN vs. LO INPUT FREQUENCY


LO LEAKAGE AT IF PIN vs. LO INPUT FREQUENCY


LO LEAKGE AT RF PIN vs. LO INPUT FREQUENCY


## PACKAGE DIMENSIONS

6 pin super minimold (Unit: mm)


## NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (example: 1000 pF ) to the Vcc pin.

## RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
| :--- | :--- | :---: |
| Infrared Reflow | Package peak temperature: $235^{\circ} \mathrm{C}$ or below <br> Time: 30 seconds or less (at $210^{\circ} \mathrm{C}$ ) <br> Count: 3, Exposure limit: None $^{\text {Note }}$ | IR35-00-3 |
| VPS | Package peak temperature: $215^{\circ} \mathrm{C}$ or below <br> Time: 40 seconds or less (at $200^{\circ} \mathrm{C}$ ) <br> Count: 3, Exposure limit: None ${ }^{\text {Note }}$ | VP15-00-3 |
| Wave Soldering | Soldering bath temperature: $260^{\circ} \mathrm{C}$ or below <br> Time: 10 seconds or less <br> Count: 1, Exposure limit: None ${ }^{\text {Note }}$ | WS60-00-1 |
| Partial Heating | Pin temperature: $300^{\circ} \mathrm{C}$ <br> Time: 3 seconds or less (per side of device) <br> Exposure limit: None ${ }^{\text {Note }}$ |  |

Note After opening the dry pack, keep it in a place below $25^{\circ} \mathrm{C}$ and $65 \% \mathrm{RH}$ for the allowable storage period.

## Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).


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